REMARKS

OVERVIEW

Claims 1-13, 15-18, and 20-25 are pending in this application. The present response is in earnest effort to place the application in proper form for allowance.

ISSUES UNDER 35 U.S.C. § 112

The Office Action of October 23, 2002 rejects claims 1-18 and 20-25 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. In particular, it was indicated that "it is not clear if stacking is required due to the limitation of 'when the resistors are stacked' and similarly, it is not clear how the encapsulant is between the top and bottom resistors of the first and second resistors if there is no stacking. Claim 14 is redundant since glass is already claimed in the base claim 9. In claim 18, a stacked resistor is claimed, but the claim also includes the components are capable of being aligned and stacked, so that it is not clear if stacking is required or what is meant." Claim 14 has been cancelled, rendering that rejection moot. The claims are intended to be directed towards a device having resistors that are stacked. Amendment has been made to clarify this point and remedy these rejections. In particular, in claim 1, the language of "separating the first film resistor and the second film resistor when the resistors are stacked" has been deleted. In claim 7, the language "separating the second film resistor and the third film resistor when the resistors are stacked" has been deleted. In claim 8, the language "separating the third film resistor and the fourth film resistor when the resistors are stacked" has been deleted. In claim 9, the language "for separating the first film resistor and the second film resistor when the resistors are stacked" has been deleted. In claim 16, the language "separating the second film resistor and third film resistor when the resistors are stacked" has

been deleted. In claim 17, the language "separating the third film resistor and the fourth film resistor when the resistors are stacked" has been deleted. In claim 18, the language "the first chip resistor and the second chip resistor capable of being aligned and stacked" has been deleted, as well as the language of "for separating the chip resistors, the layer of glass." In claim 24, the language "the third chip resistor capable of being aligned and stacked with the first chip resistor and the second chip resistor" has been deleted. And, "for separating the second chip resistor and the third chip resistor" has also been deleted. In claim 25, the language "the fourth chip resistor capable of being aligned and stacked with the first chip resistor" and "for separating the third chip resistor and the fourth chip resistor" have been deleted. The purpose of this language was to indicate that the encapsulant is not being used to bond the film resistors, but is placed between the film resistors. In addition, to further clarify that stacking is required, additional language has been added to the claims to indicate that the metal barriers are used for "mechanically bonding the film resistors without adhesive." This language has been added in independent claims 1, 9, and 18. Therefore, it is clear that the resistors must be stacked. Therefore, these rejections should be withdrawn.

ISSUES UNDER 35 U.S.C. § 102

Claim 9 has been rejected under 35 U.S.C. § 102(b) as being anticipated by Kita et al. (JP 2-270302). The Office Action of October 23, 2002 indicates at numbered paragraph 4 that "Kita discloses the invention at Figs. 3 or 4 where stacked film resistors 3 have an encapsulant depicted with first and second metal barriers 4 or 15, although the first and second barriers are joined together to form a magazine. Element 1 appears to be a glass covering for the resistor thereunder."

Kita places chip resistors within a magazine such that they can be picked out one by one. Thus, Kita is not directed towards solving the same problems as the Applicant's invention. Kita is concerned with preventing chip resistors from sticking together instead of stacking chip resistors in a single device to increase power dissipation while maintaining electrical stability and reducing board space.

The magazine of Kita is not a single device, but multiple resistors in a stacked relationship. It is submitted that the amendment to the claims to overcome the 112 rejection, also makes clear that Kita cannot anticipate. In particular, the nickel/metal barrier of the present invention provides for "mechanically bonding the film resistors without adhesive." Kita does not disclose this bonding by the metal barriers. Therefore, this rejection to claim 9 should appropriately be withdrawn.

Claims 1-18 and 20-25 have been rejected under 35 U.S.C. § 102(e, b) as being anticipated by U. S. Patent No. 6,150,920 to Hashimoto et al. or U. S. Patent No. 5,757,076 to Kambara. The Office Action of October 23, 2002, at numbered paragraph 5, indicates that the Applicant's claims do not require stacking. It is submitted that the amendment made to overcome the 112 rejections makes clear that stacking is required. In particular, language of "mechanically bonding" by the nickel/metal barriers makes clear that the resistors are stacked. Furthermore, neither Hashimoto nor Kambara disclose this stacking with nickel/metal barriers being used to mechanically bond the resistors without use of adhesive. Therefore, it is respectfully submitted that these rejections should also be appropriately be withdrawn.

Alternatively, claims 1-18 and 20-25 have been rejected under 35 U.S.C. § 103(a) as being obvious over Hashimoto or Kambara, in view of Kita (JP 2-270302) or JP 6283301. These rejections assumed stacking. JP '301 does not appear to disclose the encapsulant of the present

invention. The encapsulant of the present invention is not used to adhere the film resistors as the adhesives or epoxies are in JP '301 (see machine translation, paragraph 9). The disadvantage of using epoxy or other resins is described in the application as originally filed in the paragraph that spans pages 1 and 2. The JP '301 reference does not disclose using the encapsulant in this manner. Furthermore, the independent claims 1, 9, and 18 make clear that the metal/nickel barrier is being used for "mechanically bonding the film resistors without adhesive." JP '301 would disclose use of an adhesive, thereby teaching away from the Applicant's claimed invention.

The JP 6283301 reference does not appear to disclose an encapsulant between each film resistor in a stacked resistive device. The deficiencies of Kita, Hashimoto, and Kambara have already been discussed. There is no motivation or suggestion to combine these references to result in the Applicant's claimed invention. In particular, these references are not directed towards increasing power dissipation while maintaining electrical stability in a chip resistor by placing an encapsulant between resistors within the stacked device and connecting the end cap of different resistors through using a metal barrier that mechanically bonds the film resistors together without using adhesives. Therefore, it is respectfully submitted that these rejections are properly overcome, should be removed, and the claims should be allowed.

Claims 1-4, 7-9 and 18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over JP 6283301 in view of Hashimoto JP (4-214601). In making this rejection, the Office Action at numbered paragraph 7, equates the "encapsulant" of the Applicant's claimed invention with the "adhesives" noted on page 2 of the machine translation of the JP '301 reference. The language of the claims now makes clear that the film resistors are mechanically bonded together with the metal barriers and "without adhesive." The encapsulant of claims is not

used as an adhesive as that could result in an electrical instability effect over time due to the effects of resistive heating (see application as filed, paragraph spanning pages 1 and 2). Therefore, this rejection should be withdrawn. As the encapsulant is not adhesive, this rejection should be withdrawn.

SUMMARY

No fees or extensions of time are believed to be due in connection with this amendment; however, consider this a request for any extension inadvertently omitted, and charge any additional fees to Deposit Account No. 26-0084.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Examiner is respectfully invited to call the undersigned attorney at (515) 288-3667 to discuss the claims in an effort to reach a mutual agreement with respect to claim limitation and scope in the present application if the Examiner does not find all claims in condition for immediate allowance.

Respectfully submitted,

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Application No. 09/811,844

AMENDMENT — VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims

Please cancel claim 14.

Kindly amend claims 1, 7, 8, 9, 16, 17, 18, 24, and 25 as follows:

1. (Twice Amended)

A power chip resistor comprising:

a first and second film resistor each having (a) a substrate with a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface and an opposing side surface, (b) a film resistive element on the top surface of each substrate, (c) an end cap on the first end surface and electrically connected to the film resistive element, and (d) a second end cap on the opposing end surface and electrically connected to the film resistive element;

the second film resistor of approximately the same physical size as the first film resistor, the second film resistor of approximately the same orientation as the first film resistor;

an encapsulant between the top surface of the first film resistor and the bottom surface of the second film resistor~~, separating the first film resistor and the second film resistor when the resistors are stacked~~;

a first nickel barrier connecting the end cap on the first end surface of the first film resistor and the first end surface of the second film resistor and mechanically bonding the film resistors without adhesive;

a second nickel barrier connecting the second end cap on the second end surface of the first film resistor and the second end cap on the second end surface of the second film resistor and mechanically bonding the film resistors without adhesive.

7. (Twice Amended)

The power chip resistor of claim 1 further comprising:

a third film resistor having (a) a substrate with a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface and an opposing side surface, (b) a film resistive element on the top surface of the substrate, (c) an end cap on the first end surface electrically connected to the film resistive element, and (d) a second end cap on the opposing end surface and electrically connected to the film resistive element; a second encapsulant between the top surface of the substrate of the second film resistor and the bottom surface of the substrate of the third film resistor~~, separating the second film resistor and the third film resistor when the resistors are stacked~~, the first nickel barrier electrically connected to the end cap of the first end surface of the third film resistor, the second nickel barrier electrically connected to the second end cap on the second end surface of the third film resistor.

8. (Twice Amended)

The power chip resistor of claim 7 further comprising:

a fourth film resistor having (a) a substrate with a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface and an opposing side surface, (b) a film resistive element on the top surface of the substrate, (c) an end cap on the first end surface electrically connected to the film resistive element, and (d) a second end cap on the opposing end surface and electrically connected to the film resistive element; a third encapsulant between the top surface of the substrate of the third film resistor and the bottom surface of the substrate of the fourth film resistor~~, separating the third film resistor and the fourth film resistor when the resistors are stacked~~, the first nickel barrier electrically connected to the end cap of the first end surface of the fourth film resistor, the second nickel barrier electrically connected to the second end cap on the second end surface of the fourth film resistor.

9. (Twice Amended)

A power chip resistor comprising:

a first and second film resistor each having (a) a substrate with a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface and an opposing side surface, (b) a film resistive element on the top surface of each substrate, (c) an end cap on the first end surface of each surface electrically connected to the film resistive element, and (d) a second end cap on the opposing end surface of each substrate and electrically connected to the film resistive element; a glass encapsulant between the top surface of the substrate of the first film resistor and the bottom surface of the substrate of the second film resistor ~~for separating the first film resistor and the second film resistor when the resistors are stacked~~;

a first metal barrier covering the end caps on the first end surface of the substrate of the first and second film resistors and mechanically bonding the film resistors without adhesive;

a second metal barrier covering the second end caps on the opposing end surface of the substrate of the first and second film resistors and mechanically bonding the film resistors without adhesive.

16. (Twice Amended)

The power chip resistor of claim 9 further comprising:

a third film resistor having (a) a substrate with a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface and an opposing side surface, (b) a film resistive element on the top surface of the substrate, (c) an end cap on the first end surface electrically connected to the film resistive element, and (d) a second end cap on the opposing end surface and electrically connected to the film resistive element;

a second encapsulant between the top surface of the substrate of the second film resistor and the bottom surface of the substrate of the third film resistor~~, separating the second film resistor and the third film resistor when the resistors are stacked~~, the first nickel barrier electrically connected to the end cap of the first end surface of the third film resistor, the second nickel barrier electrically connected to the second end cap on the second end surface of the third film resistor.

17. (Twice Amended)

The power chip resistor of claim 16 further comprising:

a fourth film resistor having (a) a substrate with a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface and an opposing side surface, (b) a film resistive element on the top surface of the substrate, (c) an end cap on the first end surface electrically connected to the film resistive element, and (d) a second end cap on the opposing end surface and electrically connected to the film resistive element; a third encapsulant between the top surface of the substrate of the third film resistor and the bottom surface of the substrate of the fourth film resistor~~, separating the third film resistor and the fourth film resistor when the resistors are stacked~~, the first nickel barrier electrically connected to the end cap of the first end surface of the fourth film resistor, the second nickel barrier electrically connected to the second end cap on the second end surface of the fourth film resistor.

18. (Twice Amended)

A stacked chip resistor comprising:

a first chip resistor and a second chip resistor, each chip resistor having a substrate with a thick film resistive element attached to the substrate, a first end cap and a second end cap, each end cap being an electrical terminal connected to the thick film resistive element~~, the first chip resistor and the second chip resistor capable of being aligned and stacked~~;

a layer of glass ~~for separating the chip resistors, the layer of glass~~ placed between the first chip resistor and the second chip resistor;

a first nickel barrier, the nickel barrier electrically connecting the first end cap of the first chip resistor and the first end cap of the second chip resistor;

a second nickel barrier, the nickel barrier electrically connecting the second end cap of the first chip resistor and the second end cap of the second chip resistor~~.~~;

the nickel barriers bonding the chip resistors without adhesive.

24. (Twice Amended)

The stacked chip resistor of claim 18 further comprising:

a third chip resistor, the third chip resistor having a substrate with a thick film resistive element attached to the substrate, a first end cap and a second end cap, each end cap being an electrical terminal connected to the thick film resistive element, ~~the third chip resistor capable of being aligned and stacked with the first chip resistor and the second chip resistor~~;

a second layer of glass ~~for separating the second chip resistor and the third chip resistor, the second layer of glass~~ placed between the second chip resistor and the third chip resistor, the first nickel barrier electrically connected to the first end cap of the third chip resistor, the second nickel barrier electrically connected to the second end cap of the third chip resistor.

25. (Twice Amended)

The stacked chip resistor of claim 24 further comprising:

a fourth chip resistor, the fourth chip resistor having a substrate with a thick film resistive element attached to the substrate, a first end cap and a second end cap, each end cap being an electrical terminal connected to the thick film resistive element, ~~the fourth chip resistor capable of being aligned and stacked with the first chip resistor,~~ the second chip resistor, and the third chip resistor;

a third layer of glass ~~for separating the third chip resistor and the fourth chip resistor, the third layer of glass~~ placed between the third chip resistor and the fourth chip resistor, the first nickel barrier electrically connecting the first end cap of the fourth chip resistor with the fist end cap of the first chip resistor and the first end cap of the second chip resistor and the first end cap of the third chip resistor, the second nickel barrier electrically connected to the second end cap of the fourth chip resistor.